IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Steven T. Mayer; Vijay Bhaskaran; Evan E. Patton; Robert L. Jackson; Jonathan Reid

Assignee: Novellus Systems, Inc.

Title: Process For Electroplating Metals Into Microscopic Recessed Features

Serial No.:	09/716,016	Filing Date:	November 16, 2000
Examiner:	Unknown	Group Art Unit:	Unknown
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San Jose, California
April 16, 2001

BOX NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please enter the following amendments before taking action on the merits of the above referenced divisional application. In accordance with 37 CFR § 1.121 (a)(1), Attachment A provides marked up versions of the specification containing the newly introduced changes.

IN THE SPECIFICATION

Please replace the paragraph on page 3, lines 7-17 with the following paragraph.

One challenge facing dual damascene processing techniques noted above is the difficulty of initiating the growth of the metal film within recessed features without forming voids or seams. In typical PVD and some CVD processes, metal may preferentially deposit near the top of recessed features leading to a "bottleneck" shape. Further plating of metal onto the bottleneck may result in sealing the top of the feature before completely filling the feature with metal, creating thereby a void. Voids increase the resistance of the conductor over its designed value due to the absence of planned-for conductor. Also, trapped electrolyte sealed in voids may corrode the copper. This may lead to degraded device performance or

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